Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5580-03000 APPLICANT: Rogenmoser, et al. FILING DATE: May 4, 2001	SERIAL NO. 09/849,052 GROUP: 2124

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	5,369,607	11/29/94	Okamoto			
	A2	4,922,446	5/1/90	Zurawski, et al.			
	A3	5,867,407	2/2/99	Wolrich, et al.			
	A4	5,920,493	7/6/99	Lau			
	A5	5,957,997	9/28/99	Olson, et al.			
	A6	6,085,208	7/4/00	Oberman, et al.			

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A7	E. Hokenek and R. K. Montoye, "Leading-zero anticipator in the IBM RS/6000 floating-point execution unit," IBM Journal of Research and Development, vol. 34, no. 1, pp. 71-77, January 1990.
	A8	N. T. Quach and M. J. Flynn, "Leading one prediction - implementation, generalization, and application," Technical Report No. CSL-TR-91-463, Computer Systems Laboratory, Stanford University, March 1991.
	A9	Bruguera, et al., "Leading-One Prediction with Concurrent Position Correction," IEEE, Vol. 48, No. 10 October 1999, 8 pages.
	A10	Suzuki, et al., "Leading-Zero Anticipatory Logic for High-Speed Floating Point Addition," IEEE, Vol. 31, No. 8, August 1996, 4 pages.
	A11	SiByte, "Target Applications," http://sibyte.com/mercurian/applications.htm, January 15, 2001, 2 pages.
	A12	SiByte, "SiByte Technology," http://sibyte.com/mercurian/technology.htm, January 15, 2001, 3 pages.
	A13	SiByte, "The Mercurian Processor," http://sibyte.com/mercurian, January 15, 2001, 2 pages.
	A14	SiByte, "Fact Sheet," SB-1 CPU, October 2000, rev. 0.1, 1 page.
	A15	SiByte, "Fact Sheet," SB-1250, October 2000, rev. 0.2, 10 pages.
	A16	Stepanian, SiByte, "SiByte SB-1 MIPS64 CPU Core, Embedded Processor Forum 2000, June 13, 2000, 15 pages.
	A17	Jim Keller, "The Mercurian Processor: A High Performance, Power-Efficient CMP for Networking," October 10, 2000, 22 pages.

EXAMINER: D. H. Malzahn DATE CONSIDERED: 3/25/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

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DH	B1	Tom R. Halfhill, "SiByte Reveals 64-Bit Core For NPUs; Independent MIPS64 Design Combines Low Power, High Performance," Microdesign Resources, June 2000, Microprocessor Report, 4 pages.

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